What is claimed is:

1. A memory cell comprising:

a first inverter comprising a pull-up transistor, the pull-up transistor comprising a body terminal;

a second inverter cross-coupled to the first inverter and comprising a pull-up transistor comprising a body terminal; and

a switch connected to the bodies terminals.

2. The memory cell as set forth in claim 1, the memory cell further comprising a power rail and a ground rail, wherein

the pull-up transistor of the first inverter is a pFET, further comprising a source terminal connected to the power rail, a gate terminal, and a drain terminal;

the first inverter further comprises a pull-down nFET comprising a drain terminal connected to the drain terminal of the pFET of the first inverter, comprising a gate terminal, and comprising a source terminal connected to the ground rail;

the pull-up transistor of the second inverter is a pFET, further comprising a source terminal connected to the power rail, a gate terminal, and a drain terminal;

the second inverter further comprises a pull-down nFET comprising a drain terminal connected to the drain terminal of the pFET of the second inverter, comprising a gate terminal, and comprising a source terminal connected to the ground rail; and

wherein the gates of the pFET and the nFET of the first inverter are connected to the drain of the pFET of the second inverter, and the gates of the pFET and the nFET of the second inverter are connected to the drain of the pFET of the first inverter.

3. A memory cell comprising:

a first inverter comprising a pull-up transistor, the pull-up transistor comprising a body;

a second inverter cross-coupled to the first inverter and comprising a pull-up transistor comprising a body; and

a switch to provide a forward body bias voltage to the bodies.

4. The memory cell as set forth in claim 3, the memory cell further comprising a power rail and a ground rail, wherein

the pull-up transistor of the first inverter is a pFET, further comprising a source terminal connected to the power rail, a gate terminal, and a drain terminal;

the first inverter further comprises a pull-down nFET comprising a drain terminal connected to the drain terminal of the pFET of the first inverter, comprising a gate terminal, and comprising a source terminal connected to the ground rail;

the pull-up transistor of the second inverter is a pFET, further comprising a source terminal connected to the power rail, a gate terminal, and a drain terminal;

the second inverter further comprises a pull-down nFET comprising a drain terminal connected to the drain terminal of the pFET of the second inverter, comprising a gate terminal, and comprising a source terminal connected to the ground rail; and

wherein the gates of the pFET and the nFET of the first inverter are connected to the drain of the pFET of the second inverter, and the gates of the pFET and the nFET of the second inverter are connected to the drain of the pFET of the first inverter.

5. A memory cell comprising:

a first inverter comprising a pull-up transistor, the pull-up transistor comprising a body; and

a second inverter cross-coupled to the first inverter and comprising a pull-up transistor comprising a body;

wherein the bodies are forward biased.

6. The memory cell as set forth in claim 5, the memory cell further comprising a power rail and a ground rail, wherein

the pull-up transistor of the first inverter is a pFET, further comprising a source terminal connected to the power rail, a gate terminal, and a drain terminal;

the first inverter further comprises a pull-down nFET comprising a drain terminal connected to the drain terminal of the pFET of the first inverter, comprising a gate terminal, and comprising a source terminal connected to the ground rail;

the pull-up transistor of the second inverter is a pFET, further comprising a source terminal connected to the power rail, a gate terminal, and a drain terminal;

the second inverter further comprises a pull-down nFET comprising a drain terminal connected to the drain terminal of the pFET of the second inverter, comprising a gate terminal, and comprising a source terminal connected to the ground rail; and

wherein the gates of the pFET and the nFET of the first inverter are connected to the drain of the pFET of the second inverter, and the gates of the pFET and the nFET of the second inverter are connected to the drain of the pFET of the first inverter.

7. A memory comprising:

a cell comprising:

a first inverter comprising a pull-up transistor comprising a body terminal and a source terminal; and

a second inverter comprising a pull-up transistor comprising a body terminal and a source terminal, wherein the first and second inverters are cross-coupled to each other;

a power rail to provide a voltage Vcc to the source terminals; and

a bias voltage generator to provide a voltage Vb to the body terminals, wherein $Vb < Vcc$.

8. The memory as set forth in claim 7, further comprising:

a switch coupled to the bias voltage generator and to the body terminals so that the bias voltage generator provides the voltage Vb to the body terminals during a read operation on the memory cell.

9. The memory as set forth in claim 8, the memory comprising a ground rail to provide a voltage Vss, where $Vss < Vb$, wherein

the pull-up transistor of the first inverter is a pFET, further comprising a gate terminal and a drain terminal;

the first inverter further comprises a pull-down nFET comprising a drain terminal connected to the drain terminal of the pFET of the first inverter, comprising a gate terminal, and comprising a source terminal connected to the ground rail;

the pull-up transistor of the second inverter is a pFET, further comprising a gate terminal and a drain terminal;

the second inverter further comprises a pull-down nFET comprising a drain terminal connected to the drain terminal of the pFET of the second inverter, comprising a gate terminal, and comprising a source terminal connected to the ground rail; and

wherein the gates of the pFET and the nFET of the first inverter are connected to the drain of the pFET of the second inverter, and the gates of the pFET and the nFET of the second inverter are connected to the drain of the pFET of the first inverter.

10. The memory as set forth in claim 7, the memory comprising a ground rail to provide a voltage Vss, where Vss < Vb, wherein

the pull-up transistor of the first inverter is a pFET, further comprising a gate terminal and a drain terminal;

the first inverter further comprises a pull-down nFET comprising a drain terminal connected to the drain terminal of the pFET of the first inverter, comprising a gate terminal, and comprising a source terminal connected to the ground rail;

the pull-up transistor of the second inverter is a pFET, further comprising a gate terminal and a drain terminal;

the second inverter further comprises a pull-down nFET comprising a drain terminal connected to the drain terminal of the pFET of the second inverter, comprising a gate terminal, and comprising a source terminal connected to the ground rail; and

wherein the gates of the pFET and the nFET of the first inverter are connected to the drain of the pFET of the second inverter, and the gates of the pFET and the nFET of the second inverter are connected to the drain of the pFET of the first inverter.

11. A system comprising:

a first die comprising a functional unit;

a second die comprising a processor, the second die distinct from the first die, the second die comprising:

a memory cell, the cell comprising:

a first inverter comprising a pull-up transistor comprising a body terminal and a source terminal; and

a second inverter comprising a pull-up transistor comprising a body terminal and a source terminal, wherein the first and second inverters are cross-coupled to each other;

a power rail to provide a voltage Vcc to the source terminals; and

a bias voltage generator to provide a voltage Vb to the body terminals, wherein $Vb < Vcc$.

12. The system as set forth in claim 11, the second die further comprising:

a switch coupled to the bias voltage generator and to the body terminals so that the bias voltage generator provides the voltage Vb to the body terminals during a read operation on the memory cell.

13. The system as set forth in claim 12, the second die further comprising a ground rail to provide a voltage Vss, where Vss < Vb, wherein

the pull-up transistor of the first inverter is a pFET, further comprising a gate terminal and a drain terminal;

the first inverter further comprises a pull-down nFET comprising a drain terminal connected to the drain terminal of the pFET of the first inverter, comprising a gate terminal, and comprising a source terminal connected to the ground rail;

the pull-up transistor of the second inverter is a pFET, further comprising a gate terminal and a drain terminal;

the second inverter further comprises a pull-down nFET comprising a drain terminal connected to the drain terminal of the pFET of the second inverter, comprising a gate terminal, and comprising a source terminal connected to the ground rail; and

wherein the gates of the pFET and the nFET of the first inverter are connected to the drain of the pFET of the second inverter, and the gates of the pFET and the nFET of the second inverter are connected to the drain of the pFET of the first inverter.

14. The system as set forth in claim 11, the second die further comprising a ground rail to provide a voltage Vss, where Vss < Vb, wherein

the pull-up transistor of the first inverter is a pFET, further comprising a gate terminal and a drain terminal;

the first inverter further comprises a pull-down nFET comprising a drain terminal connected to the drain terminal of the pFET of the first inverter, comprising a gate terminal, and comprising a source terminal connected to the ground rail;

the pull-up transistor of the second inverter is a pFET, further comprising a gate terminal and a drain terminal;

the second inverter further comprises a pull-down nFET comprising a drain terminal connected to the drain terminal of the pFET of the second inverter, comprising a gate terminal, and comprising a source terminal connected to the ground rail; and

wherein the gates of the pFET and the nFET of the first inverter are connected to the drain of the pFET of the second inverter, and the gates of the pFET and the nFET of the second inverter are connected to the drain of the pFET of the first inverter.